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EXAMINER
HUISMAN, DAVID J

ART UNIT	PAPER NUMBER
2183	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,853	TAGO ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-18 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #2. IDS as received on 9/20/2000, #3. Priority Papers as received on 9/20/2000, and #4. Change of Address as received on 11/27/2002.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The abstract of the disclosure is objected to because it is too lengthy. Correction is required. See MPEP § 608.01(b). Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

6. The disclosure is objected to because of the following informalities: On page 1, line 5, replace "Filed" with --Field--. On page 17, line 10, replace "schmematic" with --schematic--. On page 21, line 18, replace "C" with --C2--. On page 28, line 26, and on page 30, line 9, replace "5" with --6--. On page 34, insert a period at the end of line 3. On page 49, line 11, replace "fetches" with --fetch--.

7. In general, the disclosure was not totally clear to the examiner. The language combined with the drawings made the overall application difficult to understand.

Appropriate correction is required.

Drawings

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Reference number 24 in Fig.1 is not mentioned within the disclosure. Reference label CHM is not mentioned within the disclosure for Fig.14. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

9. The drawings are objected to because the label "S7b" in Fig.15 should be changed to --S76--. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

10. In general, several of the drawing were quite hard to understand given the description within the specification. For instance, the routes (1), (2), (3), and (4) in Fig.4, are not totally clear. In addition, Fig.6-8 and Fig.11, are very hard to understand with all of the ovals and arrows. These figures should be illustrated more clearly for easier understanding. Also, it is still unclear as to why branch instructions include a second (C) stage, as shown in Fig.5, for instance. The examiner cannot seem to find its explanation within the disclosure. Appropriate changes should be made.

Claim Objections

11. Claim 2 recites the limitation "the first instruction sequence" on page 76, line 2, the limitation "the first or second instruction buffer" on page 76, lines 3-4, the limitation "the next branching instruction" on page 76, lines 11-12, and the limitation "the first or second branch target address information buffer" on page 76, lines 13-14 and 17-18. There is insufficient antecedent basis for these limitations in the claim. Also, in claim 2, "buffer" should be replaced with --buffers-- in lines 4, 14, and 18, on page 76.

12. Claim 3 recites the limitation "the third instruction sequence" on page 77, line 12. There is insufficient antecedent basis for these limitations in the claim. Also, in claim 3, "buffer" should be replaced with --buffers-- in line 4 on page 76, and lines 15, 17, 22, and 26, on page 77. Also, the first paragraph of claim 3 seems to be claiming the same thing as the last three paragraphs in claim 2. It is not clear whether this is desired by Applicant or a mistake.

13. Claim 4 recites the limitation "the fourth instruction sequence" on page 78, line 20. There is insufficient antecedent basis for these limitations in the claim. Also, in claim 4,

"buffer" should be replaced with --buffers-- in lines 4, 8, 23, and 26 on page 78, and line 3 on page 77. Also, the first paragraph of claim 4 seems to be claiming the same thing as the last three paragraphs in claim 2. It is not clear whether this is desired by Applicant or a mistake.

14. Claim 7 recites the limitation "the branching prediction information" on page 80, line 27, to page 81, line 1. There is insufficient antecedent basis for these limitations in the claim.

15. Claim 12 is objected to because of the following minor informalities: The word "sequences" should be replaced with --sequence-- in lines 25 and 26, on page 82.

16. Claim 13 recites the limitation "the instruction fetch" in the last two lines. There is insufficient antecedent basis for these limitations in the claim since stopping "the instruction fetch" could be interpreted as stopping the instruction fetch in the predicted branching direction or stopping the instruction fetch in the non-predicted branching direction.

17. Claim 14 recites the limitation "said target side instruction" in line 9 on page 84. There is insufficient antecedent basis for these limitations in the claim since claim 12 makes no mention of a target side instruction. Instead, a target side instruction sequence is mentioned. Furthermore, claim 14 recites the limitation "the instruction fetch" in the lines 10-11 on page 84. There is insufficient antecedent basis for these limitations in the claim since stopping "the instruction fetch" could be interpreted as stopping the instruction fetch in the predicted branching direction or stopping the instruction fetch in the non-predicted branching direction

18. Claim 16 is objected to because of the following minor informalities: The word "sequences" should be replaced with --sequence-- in lines 22 and 23, on page 84. Also, in claim 16, on page 85, lines 12-13, the phrase "if said branching instruction has been determined" should be modified so that it is clear that the branching instruction's direction is determined.

19. In general, the spacing of the words in some of the claims should be corrected. For instance, the last line of claim 18 looks is if it were one long word. Appropriate correction is required.

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

21. Claims 1, 5-9, and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiell, U.S. Patent No. 5,864,697.

22. Referring to claim 1, Shiell has taught an information processing device which reads, buffers, decodes and executes instructions from an instruction store portion by pipeline processing, comprising:

a) an instruction reading request portion which assigns a read address to said instruction store portion. See Fig.1 and column 6, lines 53-55, and note that the reading request portion (component 26) applies address to and reads instructions from instruction store 16i.

b) an instruction buffering portion including a plurality of instruction buffers which buffer instruction sequences read from said instruction store portion. See Fig.2 and column 7, lines 47-50, and note that the instruction buffer (component 60) comprises 16 individual instruction

buffers, where each buffer is an area used to store data temporarily and deliver it at a rate different from that at which it was received.

c) an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion. See Fig.1 and note that the execution unit can comprise decode components 28, 32, and 34, which decode buffered instructions, and execution units such as components 31, 40, and 42, which execute buffered instructions after they have been decoded.

d) a branching instruction detection portion which detects a branching instruction inside the instruction sequence read from said instruction store portion. Note that it is inherent that a branch instruction will be detected. The instruction type must be known so that it can be properly executed. Furthermore, the BTB (Fig.2, component 56) detects a branch based on a fetch address. See column 7, lines 58-62.

e) a branch target address information buffering portion including a plurality of branch target address information buffers which, when said branching instruction detection portion has detected a branching instruction, buffer the branch target address information for generating the branch target address of said branching instruction. See Fig.2, component 56, and column 2, lines 11-31. Note that this table holds (buffers) target address information (among other items) when a branch is detected.

f) when said branching instruction detection portion has detected a branching instruction, either the branch target address information of the branching instruction is stored in one of the plurality of branch target address information buffers, or the branch target instruction sequence of said branching instruction is stored in one of said plurality of instruction buffers in addition to the storing in said branch target address information buffer. See column 2, lines 11-31. Note that

when a branch is detected, branch target address information for that branch instruction is stored in one of the buffers (entries) of the branch target buffer. Also, it should be realized by Applicant that the use of the word "or" in the claim allows for anticipation by art that may only contain one of the limitations.

23. Referring to claim 5, Shiell has taught an information processing device as described in claim 1. Shiell has further taught that in response to a single instruction read request from said instruction reading request portion, a plurality of consecutive instructions from said read address are read from said instruction store portion and buffered in said instruction buffering portion. See column 6, lines 7-16. Note that instruction data fetched from a given address can contain multiple x86 instructions, which are buffered in component 60 of Fig.2 before being decoded. More specifically, see column 7, lines 47-50 and note that an instruction address addresses 16 instructions and therefore, the buffering portion has a capacity of 16.

24. Referring to claim 6, the examiner has noted that claim 6 and claim 1 have no major differences between them. Therefore, claim 6 is rejected for the same reasons set forth in the rejection of claim 1 above.

25. Referring to claim 7, Shiell has taught an information processing device as described in claim 6. Shiell has further taught that whether said branch target address information buffering portion buffers the branch target address information of said branching instruction is determined in accordance with the branching prediction information of the branching instruction which is detected by said instruction detection portion. See column 2, lines 11-31, and note that when a branch is encountered, if no dynamic prediction information for that branch exists, then an entry will be created for it in the BTB so that target address information, among other things, can be

stored. Therefore, it can be seen that the buffering portion buffers target information in accordance with branch prediction information.

26. Referring to claim 8, Shiell has taught an information processing device as described in claim 6. Shiell has further taught that whether said instruction buffering portion fetches the branch target instruction sequence of said branching instruction is determined in accordance with the branching prediction information of the branching instruction which is detected by said instruction detection portion. See column 7, lines 11-18, and note that if a branch is predicted taken, then the instruction sequence starting at the branch's target address will be fetched and buffered in order to attempt to keep the pipeline full.

27. Referring to claim 9, Shiell has taught an information processing device as described in claim 6. Shiell has further taught if said branching instruction detection portion predicts with a prescribed high level of probability that the branching instruction will not branch, said branch target address information buffering portion does not fetch the branch target instruction sequence of said branching instruction. See column 2, lines 11-31 (specifically, lines 18-21), and note that when a branch is predicted not-taken, the target address is not fetched by the BTB. Instead, the instruction at the next sequential address is fetched. The certainty of the prediction is based on a group of history bits within the BTB that provide information regarding the last "X" encounters of that particular branch. See column 8, lines 47-51. If, the branch has been taken "X" times in a row, then the BTB will generally predict with high probability that the branch will be taken again.

28. Referring to claim 11, Shiell has taught an information processing device as described in claim 6. Shiell has further taught that when the instruction buffer of said instruction buffering

portion is empty (it should be noted that whether the instruction buffer is empty or not, the following still hold true):

a) if a first branching instruction having a first branching possibility is detected by said branching instruction detection portion, a branch target instruction sequence of said first branching instruction is not fetched to said instruction buffering portion and said branch target address information buffering portion buffers the branch target address information of the first branching instruction. If the first branch instruction has a very low branching possibility and it is predicted not-taken by the BTB, then the target instruction sequence for that branch will not be fetched and buffered. Instead, the next sequential instruction is fetched. See column 2, lines 11-31 (specifically, lines 18-21). Regardless, the branch target address information buffering portion (BTB) will buffer the branch target address information such that the target address will be buffered along with the history update based on the outcome of the branch. See column 2, lines 15-22.

b) if said branching instruction detection portion has detected a second branching instruction which has a second branching possibility which is higher than said first branching possibility, a branch target instruction sequence of said second branching instruction is fetched to said instruction buffering portion. If the second branch instruction has a very high branching possibility and it is predicted taken by the BTB, then the target instruction sequence for that branch will be fetched and buffered. See column 2, lines 11-31 (specifically, lines 18-21).

29. Referring to claim 12, Shiell has taught an information processing device comprising:

a) an instruction fetch portion which fetches both a sequential side instruction sequence and a target side instruction sequence of a branch instruction. See column 2, lines 11-31. Note that if

a branch is predicted taken, the fetch portion will fetch the target side instruction sequence, whereas if the branch is predicted not-taken, then the sequential side instruction sequence will be fetched. Therefore, it can be seen that both of these sequences are fetched by the fetch unit, depending on the prediction.

b) a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion. See Fig.1 and Fig.2, and note that the fetch unit (Fig.2) controls what addresses are applied to the cache for fetching instructions.

c) a memory bus access portion which accesses said main memory. See Fig.1, components 12 which is connected to a bus that is connected to main memory.

d) an instruction buffer which buffers instructions which have been fetched. See Fig.2, component 60.

e) a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction for the branching instruction which is stored in said instruction buffer. See Fig.2, component 56.

f) if the branching direction of said branching instruction is not yet determined, said cache controller performs a memory bus access to said main memory according to a branching direction predicted by the branching prediction portion. See column 5, lines 52-54, column 7, lines 38-44, and column 7, lines 11-18. Note that when a branch prediction occurs (in this case, assume the branch is predicted taken), the target address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, may have to be accessed in order to retrieve

the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell, as applied above, in view of Shintani et al., U.S. Patent No. 4,532,589 (herein referred to as Shintani), and further in view of Nakanishi, U.S. Patent No. 5,835,754.

32. Referring to claim 2, Shiell has taught an information processing device which reads, buffers, decodes and executes instructions from an instruction store portion by pipeline processing, comprising:

a) an instruction reading request portion which assigns a read address to said instruction store portion. See Fig.1 and column 6, lines 53-55, and note that the reading request portion (component 26) applies address to and reads instructions from instruction store 16i.

b) an instruction buffering portion including a plurality of instruction buffers which buffer instruction sequences read from said instruction store portion. See Fig.2 and column 7, lines 47-50, and note that the instruction buffer (component 60) comprises 16 individual instruction buffers, where each buffer is an area used to store data temporarily and deliver it at a rate different from that at which it was received.

c) an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion. See Fig.1 and note that the execution unit can comprise decode components 28, 32, and 34, which decode buffered instructions, and execution units such as components 31, 40, and 42, which execute buffered instructions after they have been decoded.

d) a branching instruction detection portion which detects a branching instruction inside the instruction sequence read from said instruction store portion. Note that it is inherent that a branch instruction will be detected. The instruction type must be known so that it can be properly executed. Furthermore, the BTB (Fig.2, component 56) detects a branch based on a fetch address. See column 7, lines 58-62.

e) a branch target address information buffering portion including a plurality of branch target address information buffers which, when said branching instruction detection portion has detected a branching instruction, buffer the branch target address information for generating the branch target address of said branching instruction. See Fig.2, component 56, and column 2, lines 11-31. Note that this table holds (buffers) target address information (among other items) when a branch is detected.

f) Shiell has not taught that the first instruction sequence being processed is stored in either one of the first or second instruction buffers and when said branching instruction detection portion detects a branching instruction inside said first branching instruction sequence, a second instruction sequence of the branch target is stored in the other one of the first or second instruction buffers in accordance with the branch target address information of said branching instruction. However, Shintani has taught such a concept. See Fig.1A and column 5, line 58, to column 6, line 13. Note that a main stream is stored in a first instruction buffer and, upon

encountering a branch instruction, a second buffer is filled with the branch target instructions so that if the branch target path is taken, the instructions will already have been fetched from memory. This would result in saving time by not having to perform the fetch after the branch result is known. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a first and second instruction buffer for holding a first sequence of instructions and a target-side sequence of instructions.

g) Shiell in view of Shintani has not taught that the branch target address information of the next branching instruction inside said first instruction sequence is stored in either one of the first or second branch target address information buffers. However, Nakanishi has taught a system that includes multiple branch target buffers (BTBs), wherein some branch target information is stored in a first buffer and other branch target information is stored in a second buffer based on the location of the corresponding branch instruction. See Fig.6 and column 16, lines 56-62. It should be realized that this multiple BTB system is used since multiple instructions are fetched at once and it allows for making multiple branch predictions at the same time. See Fig.2 (multiple instructions fetched from cache) and column 16, lines 33-39 (multiple predictions at once). One of ordinary skill in the art would have recognized that this multiple BTB system is applicable to Shiell in view of Shintani's system since Shiell fetches multiple instructions at once. See column 6, lines 7-16. By making more predictions in parallel as opposed to serially, time can be saved if a first branch is not taken (and the second prediction must be used). Furthermore, since all branches have a corresponding entry in one of the two BTBs, it is inherent that a next branch instruction from the first sequence would be stored in one of the first or second BTBs. As a result it would have been obvious to one of ordinary skill in the art at the time of the invention to

implement multiple BTBs and have the next branch instruction information be stored in one of the first or second BTBs.

h) Shiell in view of Shintani has not taught the branch target address information of the branching instruction inside said second instruction sequence is stored in the other one of said first or second branch target address information buffers. However, as described above, Nakanishi has taught a system that includes multiple branch target buffers (BTBs), wherein some branch target information is stored in a first buffer and other branch target information is stored in a second buffer based on the location of the corresponding branch instruction. See Fig.6 and column 16, lines 56-62. It should be realized that this multiple BTB system is used since multiple instructions are fetched at once and it allows for making multiple branch predictions at the same time. See Fig.2 (multiple instructions fetched from cache) and column 16, lines 33-39 (multiple predictions at once). One of ordinary skill in the art would have recognized that this multiple BTB system is applicable to Shiell in view of Shintani's system since Shiell fetches multiple instructions at once. See column 6, lines 7-16. By making more predictions in parallel as opposed to serially, time can be saved if a first branch from the fetched instructions is not taken (and the second prediction must be used). Furthermore, since all branches have a corresponding entry in one of the two BTBs, it is conceivable that a branch instruction within the second sequence would have an address that results in its target information being stored in the other one of the first or second BTBs. As a result it would have been obvious to one of ordinary skill in the art at the time of the invention to implement multiple BTBs and have information corresponding to a branch instruction within the second sequence stored in the other one of the first or second BTBs.

33. Referring to claim 3, Shiell in view of Shintani and further in view of Nakanishi has taught an information processing device as described in claim 2. Furthermore, the first paragraph of claim 3 is rejected for the same reasons set forth in the rejection of claim 2(f), (g), and (h), above. In addition, Shintani has taught:

a) if the execution of the branching instruction inside said first instruction sequence has resulted in branching, said first instruction sequence and the branch target address information of the next branching instruction inside said first instruction sequence are invalidated. See column 5, line 58, to column 6, line 7. Note that if branching occurs, then the main instruction stream, which includes the next branch, is invalidated (no longer the main instruction stream) in favor of the target instruction stream. This is done by making the target-side buffer the main stream buffer (and vice-versa).

b) a third instruction sequence of the branch target of the branching instruction inside said second instruction sequence is stored in one of said first or second instruction buffers, in accordance with the branch target address information which have been stored in the other one of said first or second branch target address information buffers. Recall from part (a) above that the target-side buffer holding the second sequence of instructions is now the main stream buffer. Therefore, if a branch is detected within the second sequence, then its target instructions will be placed into the new target-side buffer (i.e., the original main stream buffer).

c) Finally, Nakanishi has taught that the branch target address information of the next branching instruction inside said second instruction sequence is stored in one of the first or second branch target address information buffers, and the branch target address information of the branching instruction inside said third instruction sequence is stored in the other one of said first or second

branch target address information buffers. It should be realized that all branches would have a place in one of the two tables and the only difference between this portion of claim 3 and claim 2(g) and (h) above is that a second sequence and third sequence are referenced instead of a first and second sequence. Therefore, this portion of claim 3 is rejected for the same reasons set forth in the rejection of claim 2(g) and (h) above.

34. Referring to claim 4, Shiell in view of Shintani and further in view of Nakanishi has taught an information processing device as described in claim 2. Furthermore, the first paragraph of claim 4 is rejected for the same reasons set forth in the rejection of claim 2(f), (g), and (h), above. In addition, Shintani has taught:

a) if the execution of the branching instruction inside said first instruction sequence has not resulted in branching, said second instruction sequence and the branch target address information of the branching instruction inside said second instruction sequence are invalidated. See column 5, line 58, to column 6, line 18. Note that if branching does not occur, then the target instruction stream, which could include a branch, is invalidated in favor of the main instruction stream. This invalidation occurs since the target path instructions are not desired for execution.

b) a fourth instruction sequence of the branch target of the next branching instruction inside said first instruction sequence is stored in one of said first or second instruction buffers, in accordance with the branch target address information which have been stored in the other one of said first or second branch target address information buffers. Recall from part (a) main stream buffer is still supplying instructions for execution. Therefore, if a next branch is detected within the first sequence, then its target instructions will be placed into the target-side buffer based on target information concerning the next branch instruction.

c) Finally, Nakanishi has taught that the branch target address information of the next branching instruction inside said first instruction sequence is stored in one of the first or second branch target address information buffers, and the branch target address information of the branching instruction inside said fourth instruction sequence is stored in the other one of said first or second branch target address information buffers. It should be realized that all branches would have a place in one of the two tables and the only difference between this portion of claim 4 and claim 2(g) and (h) above is that a second sequence and third sequence are referenced instead of a first and second sequence. Therefore, this portion of claim 4 is rejected for the same reasons set forth in the rejection of claim 2(g) and (h) above.

35. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell, as applied above, in view of Hara, U.S. Patent No. 5,740,415.

36. Referring to claim 10, Shiell has taught an information processing device as described in claim 6. Shiell has not taught that when said branch target address information buffering portion has buffered branch target address information of a first branching instruction, if said branching instruction detection portion has detected a second branching instruction which has a greater possibility of branching than said first branching instruction, said branch target address information buffering portion invalidates the branch target address information of said first branching instruction and buffers the branch target address information of said second branching instruction. However, Hara has taught such a concept. See column 9, lines 4-10. As disclosed by Hara, by storing a branch instruction having a high branch probability as opposed to an instruction with a small branch probability, branch prediction accuracy is improved. Therefore,

it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shiell's branch target address information buffer so that it operates in a manner equal to that of Hara's.

37. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell, as applied above, in view of Shintani, as applied above, and further in view of Lee et al., Instruction Cache Fetch Policies for Speculative Execution, 1995 (herein referred to as Lee).

38. Referring to claim 13, Shiell has taught an information processing device as described in claim 12.

a) Shiell has not explicitly taught fetching a sequential-side instruction sequence and a target-side instruction sequence simultaneously. However, Shintani has taught such a concept. See Fig.1A and column 5, line 58, to column 6, line 13. Note that a main stream is stored in a first instruction buffer and, upon encountering a branch instruction, a second buffer is filled with the branch target instructions so that if the branch target path is taken, the instructions will already have been fetched from memory. This would result in saving time by not having to perform the fetch after the branch result is known. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a first and second instruction buffer for holding a first sequence of instructions and a target-side sequence of instructions.

b) Shiell has taught that while the branching direction of said branching instruction is not yet determined, if the cache controller has performed a cache miss with respect to an instruction in the predicted branching direction of said branching instruction, said cache controller performs the memory bus access to the main memory for an instruction fetch. See column 5, lines 52-54,

column 7, lines 38-44, and column 7, lines 11-18. Note that when a branch prediction occurs (in this case, assume the branch is predicted taken), the target address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, may have to be accessed in order to retrieve the desired instructions, as is known in the art. This is the nature of a memory hierarchy.

c) Shiell in view of Shintani has not taught that while the branching direction of said branching instruction is not yet determined, if said cache controller has performed a cache miss with respect to an instruction which is not in the predicted branching direction, said cache controller does not perform the memory bus access and stops the instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Shiell in view of Shintani such that if said cache controller has performed a cache miss with respect to an instruction which is not in the predicted branching direction, said cache controller does not perform the memory bus access and stops the instruction fetch.

39. Referring to claim 14, Shiell has taught an information processing device as described in claim 12.

a) Shiell has not explicitly taught fetching a sequential-side instruction sequence and a target-side instruction sequence simultaneously. However, Shintani has taught such a concept. See

Fig.1A and column 5, line 58, to column 6, line 13. Note that a main stream is stored in a first instruction buffer and, upon encountering a branch instruction, a second buffer is filled with the branch target instructions so that if the branch target path is taken, the instructions will already have been fetched from memory. This would result in saving time by not having to perform the fetch after the branch result is known. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a first and second instruction buffer for holding a first sequence of instructions and a target-side sequence of instructions.

b) Shiell in view of Shintani has not taught that while the branching direction of said branching instruction is not yet determined and the predicted branching direction of said branching instruction is the sequential side, in the event of said cache controller performing a cache miss with respect to said target side instruction, said cache controller does not perform a memory bus access and stops the instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Shiell in view of Shintani such that if said cache controller has performed a cache miss with respect to said target side instruction, said cache controller does not perform a memory bus access and stops the instruction fetch.

40. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell as applied above, in view of Lee, as applied above.

41. Referring to claim 15, Shiell has taught an information processing device as described in claim 12. Shiell has not taught that while the branching direction of said branching instruction is not yet determined, said cache controller does not perform a memory bus access after a cache miss depending on the predicted branching direction of said branching instruction. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Shiell such that the cache controller does not perform a memory bus access after a cache miss depending on the predicted branching direction of said branching instruction.

42. Referring to claim 16, Shiell has taught an information processing device, comprising:
a) an instruction fetch portion which fetches both a sequential side instruction sequence and a target side instruction sequence of a branching instruction. See column 2, lines 11-31. Note that if a branch is predicted taken, the fetch portion will fetch the target side instruction sequence, whereas if the branch is predicted not-taken, then the sequential side instruction sequence will be fetched. Therefore, it can be seen that both of these sequences are fetched by the fetch unit, depending on the prediction.

b) a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion. See Fig.1 and Fig.2, and note that the fetch unit (Fig.2) controls what addresses are applied to the cache for fetching instructions.

c) a memory bus access portion which accesses said main memory. See Fig.1, components 12 which is connected to a bus that is connected to main memory.

d) an instruction buffer which buffers instructions which have been fetched. See Fig.2, component 60.

e) a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction of the branching instruction which is stored in said instruction buffer. See Fig.2, component 56.

f) if said branching instruction has been determined and said cache controller performs a cache miss with respect to an instruction in the determined branching direction, said cache controller performs a memory bus access. See column 5, lines 52-54, column 7, lines 38-44, and column 7, lines 11-18. Note that when a branch prediction occurs (in this case, assume the branch is predicted taken), the target address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, may have to be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

g) Shiell has not taught that if the branching direction of said branching instruction is not yet determined and said cache controller performs a cache miss with respect to an instruction fetch, said cache controller does not perform a memory bus access and stops the instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has

been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Shiell such that if the branching direction of said branching instruction is not yet determined and said cache controller performs a cache miss with respect to an instruction fetch, said cache controller does not perform a memory bus access and stops the instruction fetch.

43. Referring to claim 17, Shiell in view of Lee has taught an information processing device as described in claim 16. Shiell has further taught that if the branching direction of said branching instruction is not yet determined, an instruction for which a cache hit has been made is prefetched and stored in said instruction buffer. It should be realized that before a branch's direction is determined, instructions along the predicted path will be fetched from memory. If a cache hit occurs, these instruction are brought in from the cache and placed into the instruction buffer. See column 7, lines 38-44.

44. Referring to claim 18, Shiell in view of Lee has taught an information processing device as described in claim 16. Shiell has further taught that instructions are selected from either said instruction sequential side or instruction target side in said instruction buffer depending on the branching direction of the branching prediction portion, and decoded. If a branch is predicted not-taken, for instance, sequential-side instructions will be speculatively fetched, buffered, and decoded. Likewise, if a branch is predicted taken, target-side instructions will be speculatively

fetched, buffered, and decoded. Therefore, it can be seen that either sequential-side or target-side instructions will be selected from the buffer depending on the predicted branching direction.

Conclusion

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

DJH
David J. Huisman
July 30, 2003